



PMD040B

24-Bit Analog-to-Digital Converter

Datasheet

Version 0.02

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6F-6, No.1, Sec. 3, Gongdao 5th Rd., Hsinchu City 30069, Taiwan, R.O.C.

TEL: 886-3-572-8688  www.padauk.com.tw

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Revision History

| Revision | Date | Description |
|----------|------------|--|
| 0.00 | 2025/09/25 | Preliminary version |
| 0.01 | 2026/02/02 | 1. Adjust the typical value of gain drift 2. Adjust the values in the read data timing table |
| 0.02 | 2026/05/21 | 1. Section 4.1: Added operating condition for full-scale input voltage. 2. Section 4.3: Added ENOB test data. |

Usage Warning

User must read all application notes of the IC by detail before using it.

Please visit the official website to download and view the latest APN information associated with it.

https://www.padauk.com.tw/en/product/search_list.aspx?kw=PMD

1. Features

1.1. Main Features

- ◆ Supply Voltage: 3V ~ 5.5V
- ◆ Internal Programmable Gain Amplifier: 1x, 2x, 4x, 8x, 16x, 32x, 64x, 128x
- ◆ Selectable output Data Rate: 10Hz, 20Hz, 40Hz, 80Hz, 160Hz, 320Hz, 640Hz, 1280Hz
- ◆ Two-Wire Serial Digital Interface
- ◆ Power Down function
- ◆ Internal Oscillator
- ◆ Internal Temperature Sensor
- ◆ Package: SOP-8
- ◆ Operating Temperature Range: -40°C ~ 85°C

1.2. Applications

- ◆ Weigh Scales
- ◆ Load Cells
- ◆ Strain Gauge
- ◆ Instrumentation
- ◆ Precision Sensing

1.3. General Description

- ◆ The PMD040B is a 24-bit Delta-Sigma A/D converter with a differential input channel. It includes programmable gain amplifier (PGA) functions, precision 24-bit delta sigma modulator, oscillator and temperature sensor.
- ◆ The PGA has a gain option of 1x, 2x, 4x, ..., 64x, 128x. The delta-sigma ADC has 24-bit resolution and is comprised of a 2nd order modulator and 3rd digital filter. The output data rate is selectable from 10Hz, 20Hz, 40Hz,to 1280Hz.
- ◆ The PMD040B can be controlled by MCU through 2 wire SPI interfaces. It also can be put in power down mode to save power.

2. General Description and Block Diagram

The PMD040B is a low power, high precision Delta-Sigma ADC. It builds in a delta-sigma ADC, a differential input channel and a temperature sensor. This ADC uses 2nd order delta-sigma modulator and low noise instrumentation amplifier to provide maximum gain of 128x. The effective resolution with PGA gain=128x can achieve 20.5 bit while power supply is 5V.

The PMD040B has built in RC oscillator, it doesn't need external Xtal. It can be configured in multiple function through DOUT and SCLK. For example, except the high precision differential signal detection, it also can detect the temperature, setting differential PGA gain and ADC output data rate.

PMD040B also has a power switch to provide the load cell current. During normal mode, the switch is closed and the load cell current is flowing through the switch. During the power down mode, the switch is opened and it can turn off the supply current.

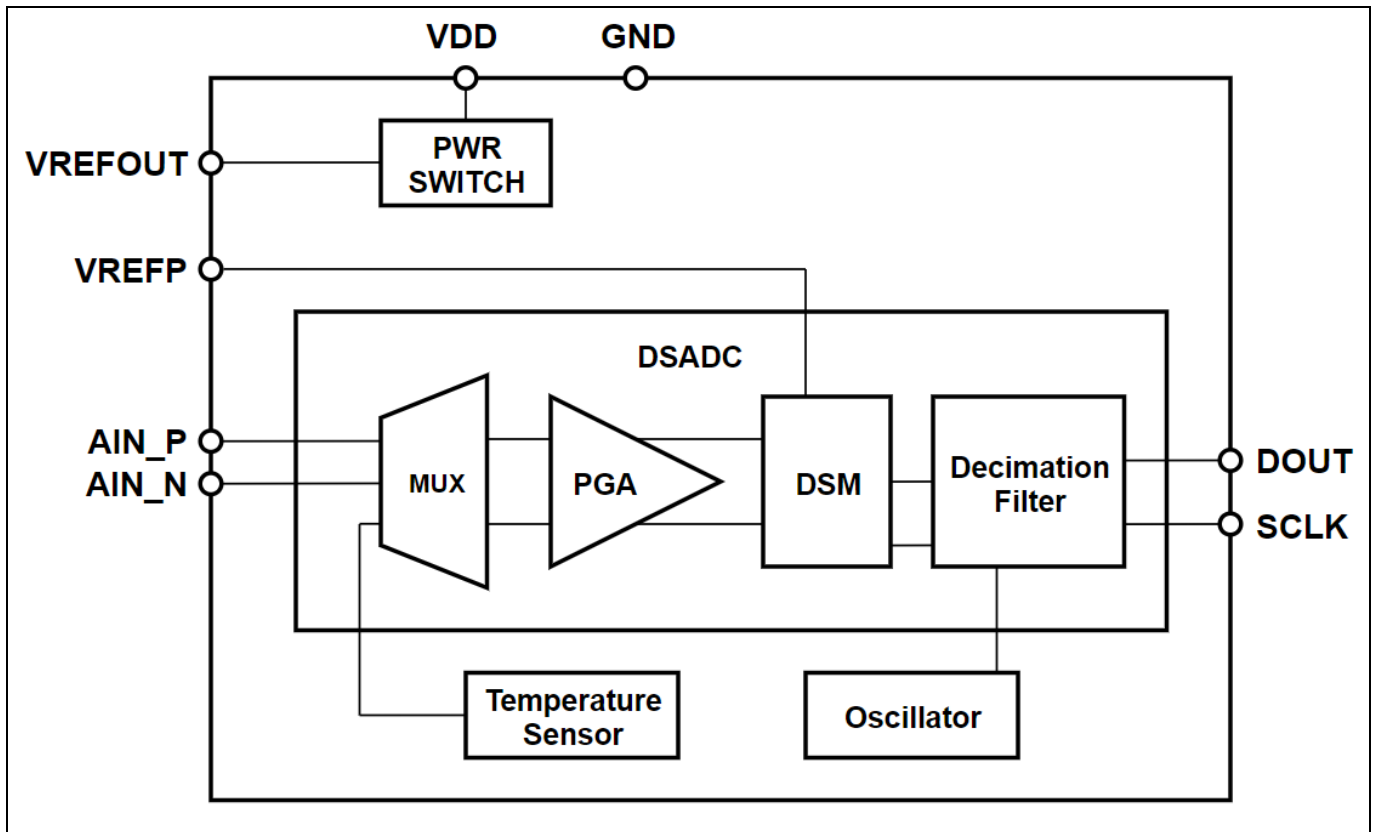
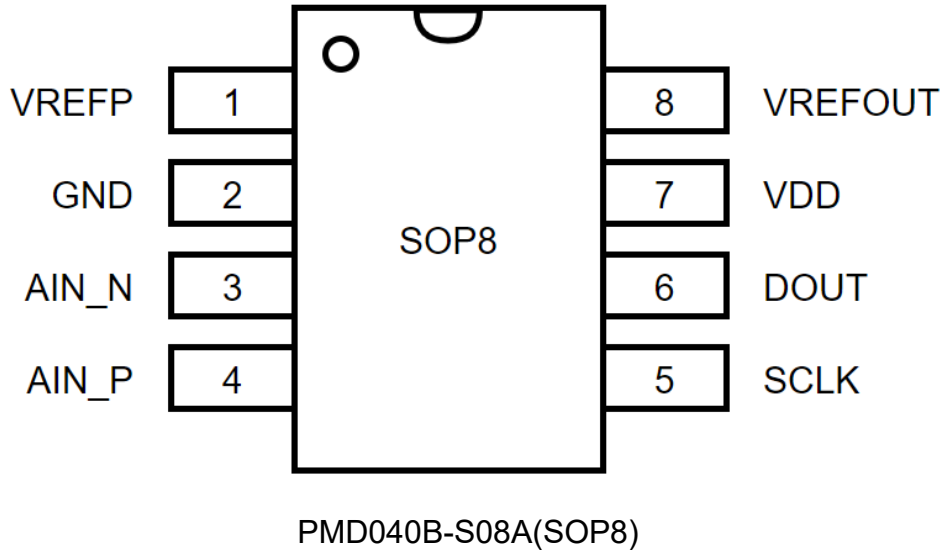


Fig.1: Block diagram of PMD040B

3. Pin Assignment and Description



| Num | PIN Name | I/O | Description |
|-----|----------|-------|-----------------------------------|
| 1 | VREFP | AI | Positive Reference Voltage |
| 2 | GND | GND | Ground |
| 3 | AIN_N | AI | Negative Analog Input |
| 4 | AIN_P | AI | Positive Analog Input |
| 5 | SCLK | DI | SPI Clock Input |
| 6 | DOUT | DI/DO | SPI Data Input / Output |
| 7 | VDD | PWR | Power Supply |
| 8 | VREFOUT | AO | Positive Reference Voltage Output |

4. Device Characteristics

4.1. Electrical Characteristics

Minimum/maximum limit specifications apply from -40°C to $+85^{\circ}\text{C}$. Typical specifications at $+25^{\circ}\text{C}$

All data are acquired under the conditions of $V_{\text{DD}}=5.0\text{V}$, unless noted.

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|-------------------------|---------|-------------------------------------|------------|------|
| POWER SUPPLY | | | | | |
| Supply Voltage | VDD | 3 | 5 | 5.5 | V |
| Supply Current (VDD=5V) | PGA=1x, 2x | | 0.85 | | mA |
| | PGA=4x-128x | | 1.50 | | mA |
| | Power down | | 0.1 | | uA |
| Supply Current (VDD=3.3V) | PGA=1x, 2x | | 0.65 | | mA |
| | PGA=4x-128x | | 1.20 | | mA |
| | Power down | | 0.1 | | uA |
| ANALOG INPUT | | | | | |
| Full scale input voltage (AINP-AINN) | | | $\pm 0.5V_{\text{REF}}/\text{Gain}$ | | |
| | VREF=VDD=5V PGA=128x | | | ± 19.5 | mV |
| | VREF=VDD=3V PGA=128x | | | ± 11.7 | mV |
| Common-mode input range** | PGA=1x, 2x | GND+0.1 | | VDD-0.1 | V |
| | PGA=4x-128x | GND+1.4 | | VDD-1.5 | V |
| Absolute input current *** | PGA=1x | | 1.2 | | nA |
| | PGA=2x | | 1.8 | | nA |
| | PGA=4x | | 3.9 | | nA |
| | PGA=128x | | 4 | | nA |
| Differential input current *** | PGA=1x | | 3 | | nA |
| | PGA=2x | | 0.75 | | nA |
| | PGA=4x | | 2.2 | | nA |
| | PGA=128x | | 0.02 | | nA |

** The specification of the common mode input range is based on the dynamic operating range of the PGA's input and the linearity of the PGA's output when the PGA's output is within the full-scale voltage range. The common mode input range is also limited by the ADC full scale output data.

*** The specification of analog input current is the simulation result.

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| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|------------------------------------|------------------|-----|------------------------------------|-----|-------------|
| SYSTEM PERFORMANCE | | | | | |
| Resolution | no missing code | | 24 | | Bits |
| Data Rate | | | 10 | | SPS |
| Digital filter settling time | | | 4 | | Conversions |
| P-P noise | DR=10, PGA=128x | | 174 (VREF=5V) | | nv, p-p |
| ENOB | DR=10, PGA=128x | | 20.5 (VREF=5V) 20.0 (VREF=3.3V) | | Bits |
| INL | PGA=128x | | ±15 | | ppm |
| Input offset error | PGA=128x | | ±5 | | uV |
| Input offset drift | PGA=128x | | ±20 | | nV/°C |
| Gain error | PGA=128x | | ±0.5 | | % |
| Gain drift | PGA=128x | | ±30 | | ppm/°C |
| VOLTAGE REFERENCE | | | | | |
| Voltage reference input (VREFP) | | 1.5 | VDD | VDD | V |
| Voltage reference output (VREFOUT) | | | VDD | | V |
| HIGH SIDE POWER SWITCH | | | | | |
| On-Resistance (Ron) | VDD=5V, Isw=20mA | | 6 | | ohm |
| | VDD=3V, Isw=20mA | | 10 | | ohm |
| Current Through Switch | | | | 20 | mA |

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| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------|---------|-------|---------|--------|
| DIGITAL INPUT/OUTPUT | | | | | |
| VIH | | 0.6*VDD | | VDD | V |
| VIL | | GND | | 0.4*VDD | V |
| VOH | IOH=1mA | VDD-0.5 | | VDD | V |
| VOL | IOL=1mA | GND | | 0.2*VDD | V |
| CLOCK | | | | | |
| OSC clock frequency | | | 5.243 | | MHz |
| OSC clock frequency drift | | | 100 | | ppm/°C |
| TEMPERATURE SENSOR | | | | | |
| Temperature Measure Error | | | ±3 | | °C |

* Specification is assured by the combination of design and final test.

4.2. Absolute Maximum Ratings

| Parameter | Maximum Rating | Notes |
|-----------------------|--------------------|--|
| Supply Voltage (VDD) | 3V ~ 6V | If VDD exceeds the maximum rating, it may cause permanent damage to the IC |
| Input Voltage | -0.3V ~ VDD + 0.3V | |
| Operating Temperature | -40°C ~ 85°C | |
| Junction Temperature | 150°C | |
| Storage Temperature | -50°C ~ 125°C | |
| Supply Voltage (VDD) | 3V ~ 6V | |

4.3. Effective Number of Bits (ENOB)

| ENOB (RMS) | VDD=5V | | | | | | | | |
|---------------|-----------|------|------|------|------|------|------|------|------|
| | Date Rate | 10 | 20 | 40 | 80 | 160 | 320 | 640 | 1280 |
| PGA Gain | x1 | 22.0 | 21.6 | 21.1 | 20.6 | 20.0 | 19.5 | 18.9 | 18.2 |
| | x2 | 22.2 | 21.6 | 21.1 | 20.6 | 20.1 | 19.6 | 19.0 | 18.4 |
| | x4 | 22.0 | 21.5 | 21.0 | 20.5 | 20.0 | 19.5 | 19.0 | 18.2 |
| | x8 | 22.0 | 21.5 | 21.0 | 20.6 | 20.0 | 19.5 | 18.8 | 18.2 |
| | x16 | 21.9 | 21.4 | 20.9 | 20.4 | 19.9 | 19.4 | 18.8 | 18.0 |
| | x32 | 21.7 | 21.3 | 20.8 | 20.3 | 19.8 | 19.3 | 18.6 | 18.0 |
| | x64 | 21.3 | 20.8 | 20.3 | 19.8 | 19.3 | 18.9 | 18.3 | 17.7 |
| | x128 | 20.6 | 20.1 | 19.6 | 19.1 | 18.6 | 18.1 | 17.6 | 17.0 |

| ENOB (RMS) | VDD=4V | | | | | | | | |
|---------------|-----------|------|------|------|------|------|------|------|------|
| | Date Rate | 10 | 20 | 40 | 80 | 160 | 320 | 640 | 1280 |
| PGA Gain | x1 | 21.6 | 21.2 | 20.7 | 20.2 | 19.6 | 19.1 | 18.7 | 17.9 |
| | x2 | 21.8 | 21.4 | 20.8 | 20.3 | 19.8 | 19.3 | 18.8 | 18.2 |
| | x4 | 21.6 | 21.2 | 20.7 | 20.2 | 19.7 | 19.1 | 18.6 | 17.9 |
| | x8 | 21.7 | 21.2 | 20.7 | 20.1 | 19.6 | 19.1 | 18.6 | 17.9 |
| | x16 | 21.6 | 21.0 | 20.6 | 20.1 | 19.6 | 19.1 | 18.5 | 18.0 |
| | x32 | 21.4 | 20.9 | 20.5 | 19.9 | 19.4 | 18.9 | 18.4 | 17.8 |
| | x64 | 21.0 | 20.5 | 20.0 | 19.5 | 19.1 | 18.6 | 18.0 | 17.4 |
| | x128 | 20.3 | 19.8 | 19.3 | 18.8 | 18.4 | 17.7 | 17.4 | 16.7 |

| ENOB (RMS) | VDD=3V | | | | | | | | |
|---------------|-----------|------|------|------|------|------|------|------|------|
| | Date Rate | 10 | 20 | 40 | 80 | 160 | 320 | 640 | 1280 |
| PGA Gain | x1 | 21.2 | 20.7 | 20.3 | 19.7 | 19.1 | 18.6 | 18.2 | 17.6 |
| | x2 | 21.3 | 21.0 | 20.4 | 19.8 | 19.4 | 18.9 | 18.4 | 17.9 |
| | x4 | 21.1 | 20.8 | 20.2 | 19.7 | 19.1 | 18.6 | 18.2 | 17.5 |
| | x8 | 21.2 | 20.7 | 20.2 | 19.7 | 19.2 | 18.7 | 18.1 | 17.5 |
| | x16 | 21.2 | 20.6 | 20.2 | 19.6 | 19.0 | 18.6 | 18.1 | 17.6 |
| | x32 | 21.0 | 20.5 | 20.0 | 19.5 | 19.0 | 18.5 | 17.9 | 17.4 |
| | x64 | 20.6 | 20.1 | 19.6 | 19.1 | 18.6 | 18.0 | 17.6 | 17.1 |
| | x128 | 19.9 | 19.4 | 18.9 | 18.4 | 17.9 | 17.4 | 16.8 | 16.3 |

5. Functional Description

The PMD040B is a precision, 24-bit ADC that includes a low-noise PGA, internal oscillator, second order delta-sigma modulator, and third order digital filter. Data can be output at 10 SPS for excellent 50Hz and 60Hz rejection or higher data rate up to 1280 SPS when higher speeds are needed.

5.1. Analog Input Front End

The input signal source of the ADC can select external differential signal from AIN_P, AIN_N or temperature sensor output signal through configuration register **cfgr1[0]**.

The PMD040B can provide different gain setting from 1x, 2x, 4x, ..., 64x, 128x. As select gain of 1x or 2x, the PGA will be turned off to save power. The analog input path will bypass PGA and only use PGA buffer to amplify the signal. As select higher gain setting, the PGA will be turned on and provide 4x to 128x gain option. The configuration register **cfgr2[0]**, **cfgr2[4]** and **cfgr2[7:5]** are used to control the gain setting.

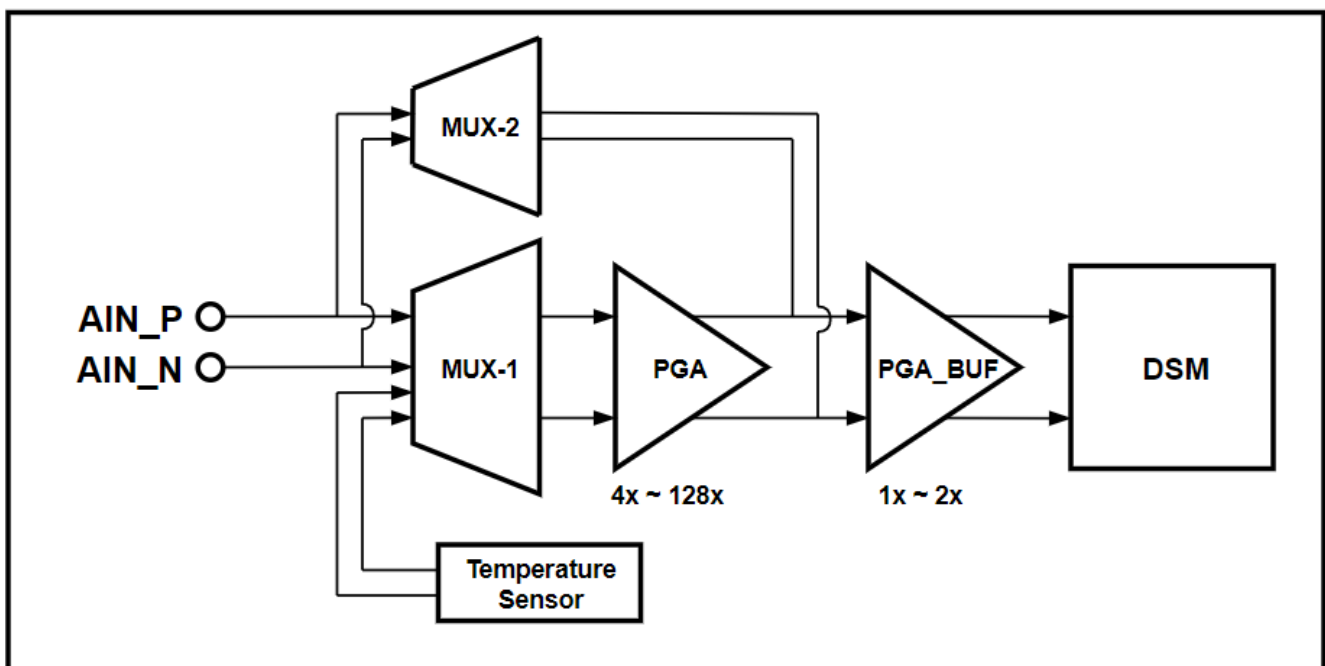


Fig. 2: Diagram of Analog input front end

5.2. Low Noise Programmable Gain Amplifier

The PMD040B features a low noise instrumentation amplifier which is suitable for bridge sensor application. The simplified diagram of the amplifier is shown in Figure 3. The low noise amplifier includes two stage amplifiers. First stage amplifier is composed of Amp1, Amp2 and RF1, RF2, R0 that provides low noise and high gain function. The gain1 option (4x~128x) can be set by cfgr2[7:5]. Second stage amplifier is a low noise buffer amplifier that provide gain2 option (1x, 2x). When PGA gain select 1x and 2x, the first stage amplifier will bypass to save power and only second stage amplifier provide 1x and 2x gain option. The table 1 lists the PGA gain option controlled by configuration register cfgr2[0], cfgr2[4], cfgr2[7:5].

The input differential channel also has a low pass filter as the EMI filter which block out unwanted higher frequency noise and also enhance the ESD performance. The cut off frequency of the EMI filter is 20MHz.

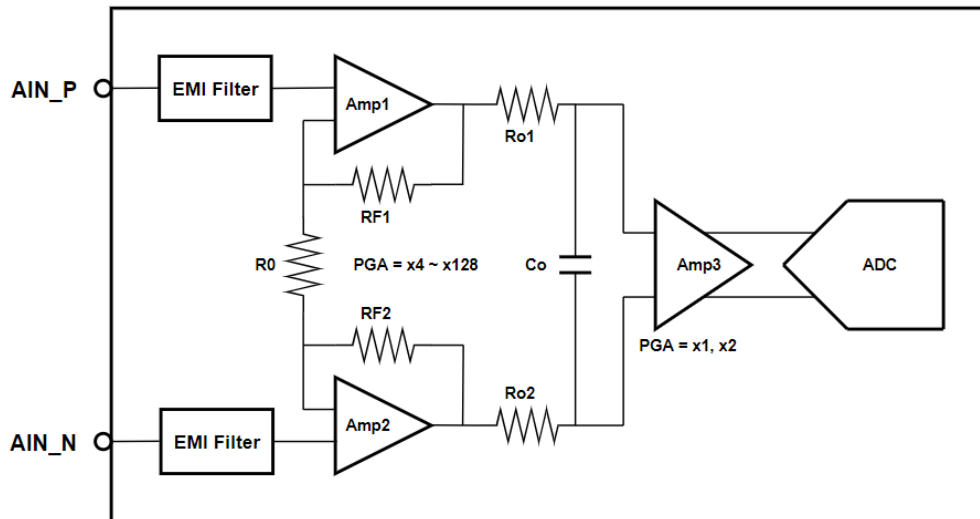


Fig.3: Diagram of Programmable Gain Amplifier

| PGA Total Gain | PGA_GSEL | | | PGABUF_GSEL | PGA_BYPASS |
|-------------------|-----------|-----------|-----------|-------------|------------|
| | cfgr2 [7] | cfgr2 [6] | cfgr2 [5] | cfgr2 [4] | cfgr2 [0] |
| 1x | - | - | - | 0 | 1 |
| 2x | - | - | - | 1 | 1 |
| 4x | 0 | 1 | 0 | 0 | 0 |
| 8x | 0 | 1 | 1 | 0 | 0 |
| 16x | 1 | 0 | 0 | 0 | 0 |
| 32x | 1 | 0 | 1 | 0 | 0 |
| 64x | 1 | 1 | 0 | 0 | 0 |
| 128x | 1 | 1 | 1 | 0 | 0 |

Table 1: PGA Gain Setting

5.3. Temperature Sensor

PMD040B provides an internal temperature sensor to measure the ambient temperature. By selecting the analog input channels to temperature sensor signals, the A/D Converter can obtain a voltage information and then use the result to derive the temperature. The temperature sensor needs to do 2 points calibration.

Calibration method:

The equation of the temperature vs temperature sensor output value is:

$$Y_x + OS = SL * (273.15 + T_x) \quad \dots\dots\dots\text{equation (1)}$$

At a certain temperature T_a , record the temperature sensor output value Y_a .

At a certain temperature T_b , record the temperature sensor output value Y_b

OS : ADC Offset

SL : ADC Slope $(Y_a - Y_b) / (T_a - T_b)$

Then, calculating from the equation (1) above, we can get

$$Y_a + OS = SL * (273.15 + T_a) \quad \dots\dots\dots\text{equation (2)}$$

$$Y_b + OS = SL * (273.15 + T_b) \quad \dots\dots\dots\text{equation (3)}$$

equation (2) / equation (3)

$$(Y_a + OS) / (Y_b + OS) = (SL * (273.15 + T_a)) / (SL * (273.15 + T_b))$$

$$Y_a * (273.15 + T_b) + OS * (273.15 + T_b) = Y_b * (273.15 + T_a) + OS * (273.15 + T_a)$$

$$OS(T_a - T_b) = Y_a * (273.15 + T_b) - Y_b * (273.15 + T_a)$$

$$OS = (Y_a * (273.15 + T_b) - Y_b * (273.15 + T_a)) / (T_a - T_b)$$

So, the ambient temperature can be calculated from equation (1) if the temperature sensor is used.

The table 2 lists the register setting while using the temperature sensor.

| TS_DIFF | TS_EN | DSADC_DR | | | MUX_SEL | |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| cfgr1 [6] | cfgr1 [5] | cfgr1 [4] | cfgr1 [3] | cfgr1 [2] | cfgr1 [1] | cfgr1 [0] |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |

Table 2: Configuration Register Setting of the Temperature Sensor.

5.4. High Side Power Switch

The PMD040B incorporates an internal switch for use with an external bridge sensor. During normal conversion, the switch is closed, the bridge sensor is powered by the switch. During standby or power-down mode, the switch is opened. By opening the switch, power dissipation in the bridge is eliminated and save the power consumption.

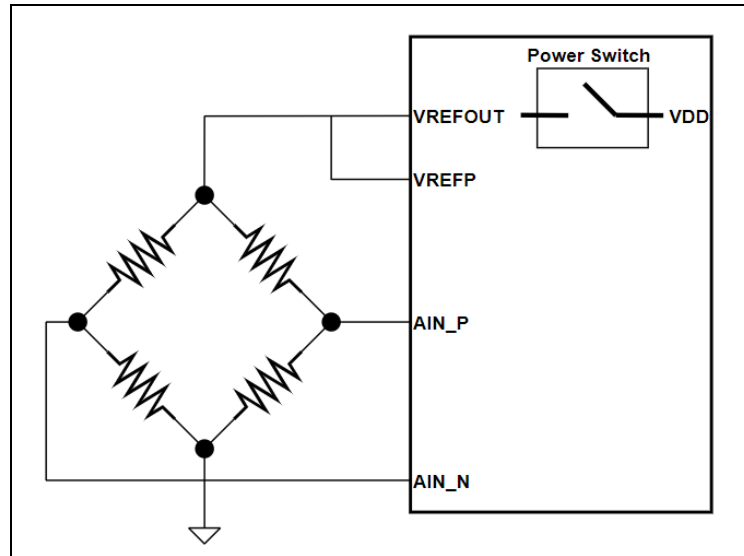


Fig. 4: Diagram of High Side Power Switch

5.5. Power Down Mode

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. When SCLK changes the state from low voltage level to high voltage level and keep the high level over 100us, the PMD040B will enter power down mode. When SCLK return to low voltage level, the chip will go back to normal mode.

When the system re-enter normal mode from power down mode, all functions are configured to the state before power down.

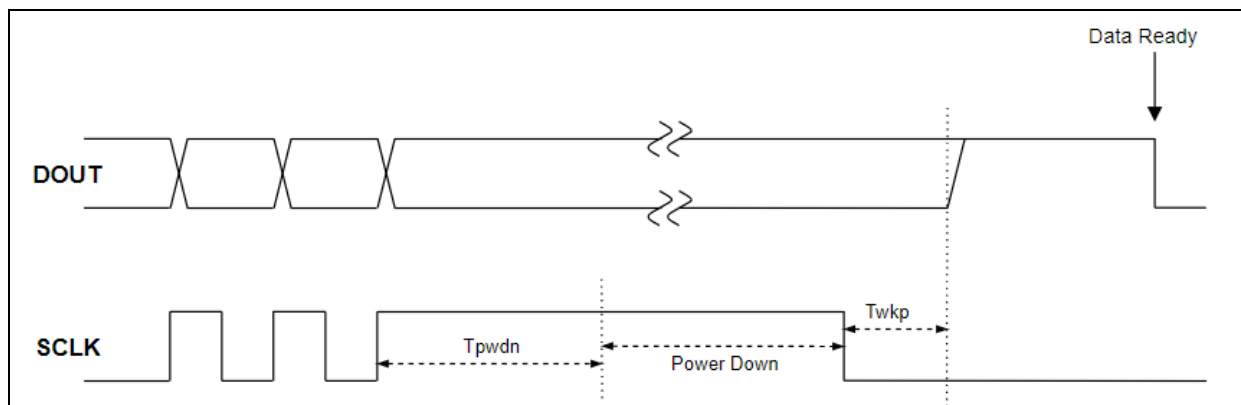


Fig. 5: Timing diagram of the Power Down Mode.

| SYMBOL | DESCRIPTION | MIN | TYP | UNITS |
|-------------------|---|-----|-----|-------|
| T _{pwdn} | Enter Power Down mode time. (SCLK hold high level time) | 100 | | us |
| T _{wkp} | Wake-up time after Power-Down mode. (SCLK hold low level time) | 10 | | us |

Table 3: Power Down mode timing table.

5.6. 2-Wire SPI communication

PMD040B adopt 2-wire SPI communication. Data reception and function configuration can be achieved through SCLK and DOUT.

5.6.1. Settling Time

The PMD040B requires 4 data conversion cycles to create correct data after power on, power down recovery and register configuration.

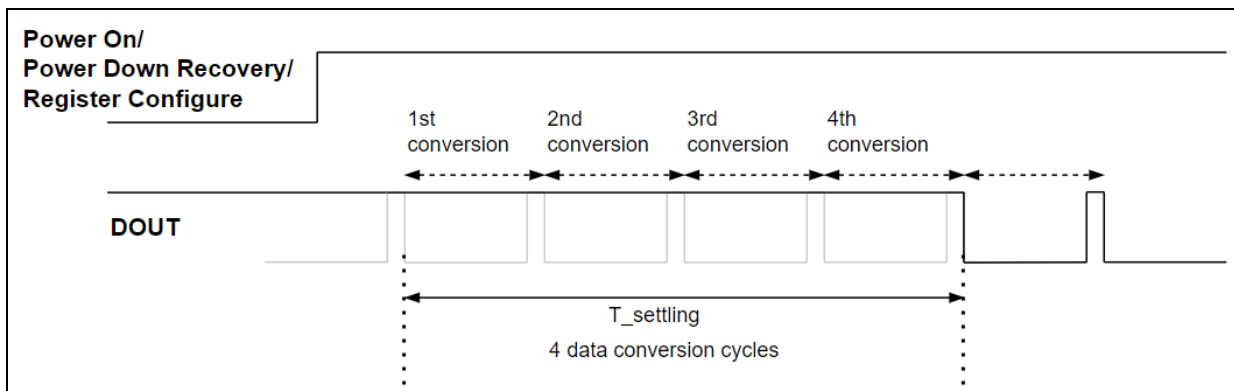


Fig. 6: Timing diagram of the data settling after power on, power down recovery and register configuration.

When PMD040B operates at the continuous conversion mode, any changes in the analog input signal also require time to settle. It requires 4 data conversion cycles to meet the settling time requirements of the analog input signal and the digital filter.

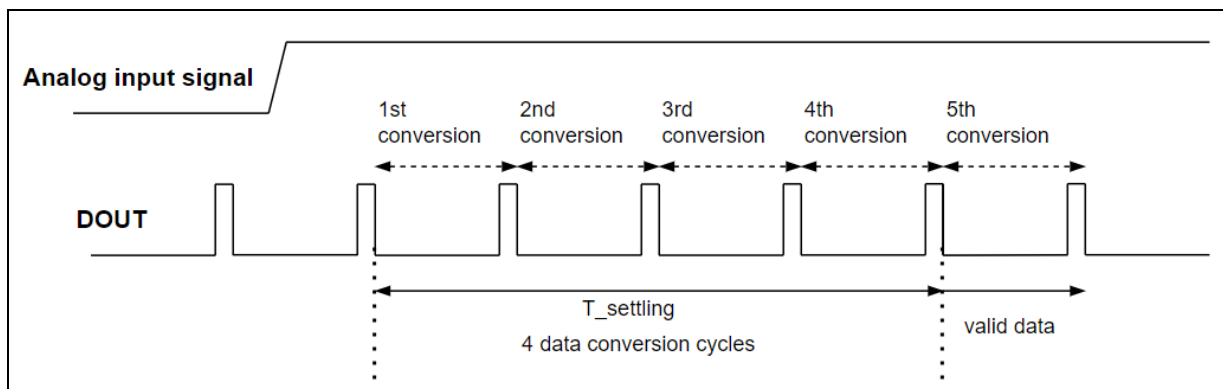


Fig. 7: Timing diagram of the data settling when analog input signal is changed.

5.6.2. Data Rate of the ADC Output

The data rate of the PMD040B can be configured through register `cfgr1` [4:2]. The default setting is 10Hz. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference.

| Data Rate | Output Data Rate Select | | |
|-----------|-------------------------|-----------|-----------|
| | cfgr1 [4] | cfgr1 [3] | cfgr1 [2] |
| 10Hz | 0 | 0 | 0 |
| 20Hz | 0 | 0 | 1 |
| 40Hz | 0 | 1 | 0 |
| 80Hz | 0 | 1 | 1 |
| 160Hz | 1 | 0 | 0 |
| 320Hz | 1 | 0 | 1 |
| 640Hz | 1 | 1 | 0 |
| 1280Hz | 1 | 1 | 1 |

Table 4: Register Setting of the output data rate.

5.6.3. Data Format

The PMD040B outputs 24 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(0.5 \cdot V_{ref}/Gain)/(2^{23}-1)$. The positive full-scale input produces an output code of 7FFFFFFh and the negative full-scale input produces an output code of 800000h. Table 4 summarizes the ideal output codes for different input signals.

| Input Signal (AINP-AINN) | Ideal Output |
|--|--------------|
| $\geq +0.5 \cdot V_{REF}/Gain$ | 7FFFFFFh |
| $(+0.5 \cdot V_{REF}/Gain)/(2^{23}-1)$ | 000001h |
| 0 | 000000h |
| $(-0.5 \cdot V_{REF}/Gain)/(2^{23}-1)$ | FFFFFFh |
| $\leq -0.5 \cdot V_{REF}/Gain$ | 800000h |

Table 5: Ideal Output Code vs Input Signal.

5.6.4. Data Ready/Data Output (DOUT)

The digital output pin-DOUT serves four purposes:

1. It indicates when new data are ready by going low.
2. After ready signal, on the first rising edge of SCLK, the DOUT pin begins outputting the conversion data, most significant (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all, 24 bits have been retrieved, If SCLK transmission is suspended at this time, DOUT will hold the last bit data until the new data is ready. Before the new data is ready, the DOUT will pull high again and then pull low while the new data conversion is completed. After that, next new data can be read on the subsequent SCLK rising edge.
3. On the 25th and 26th SCLK clock, DOUT outputs the information if the register is updated.
4. As the register data read/write pin, when it requires configuring or reading the register data, SPI need to transmit 46 SCLK clock. To determine whether it is in register write operation or read operation is based on the input command character by DOUT.

5.6.5. Serial Clock Input (SCLK)

This digital input shifts serial data out with each edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

5.6.6. Data Retrieval

The PMD040B can continuously converts the analog input signal. When the DOUT goes low, the converted data is ready to output as shown in Figure 7. ADC begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before new data are updated (within T_{conv}) or else the data will be overwritten. Avoid data retrieval during the update period (T_{update}). If only 24 SCLKs have been applied, DOUT remains at the state of the last bit shifted out until it is taken high, indicating the new data are being updated. On the 25th and 26th SCLK clock, DOUT outputs the information if the register is updated. When the DOUT corresponding to the 25th SCLK is 1, it indicates that the configuration register has been written with a new value. The DOUT corresponding to the 26th SCLK is reserved for expansion and now is always 0. DOUT can be pulled high after the 27th SCLK. After that, when DRDY/DOUT is pulled low again, it indicates that new data is ready to be output. Figure 8 shows the timing diagram of this reading procedure.

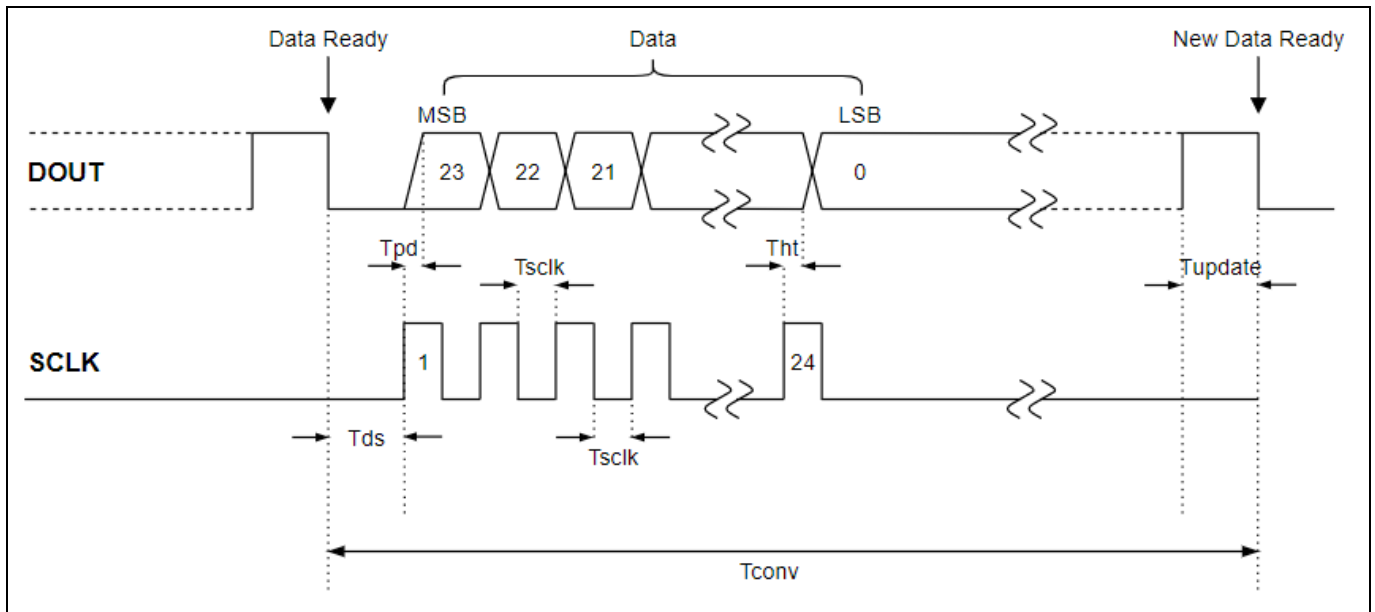


Fig. 8: Timing diagram of the reading data procedure (24 SCLKs).

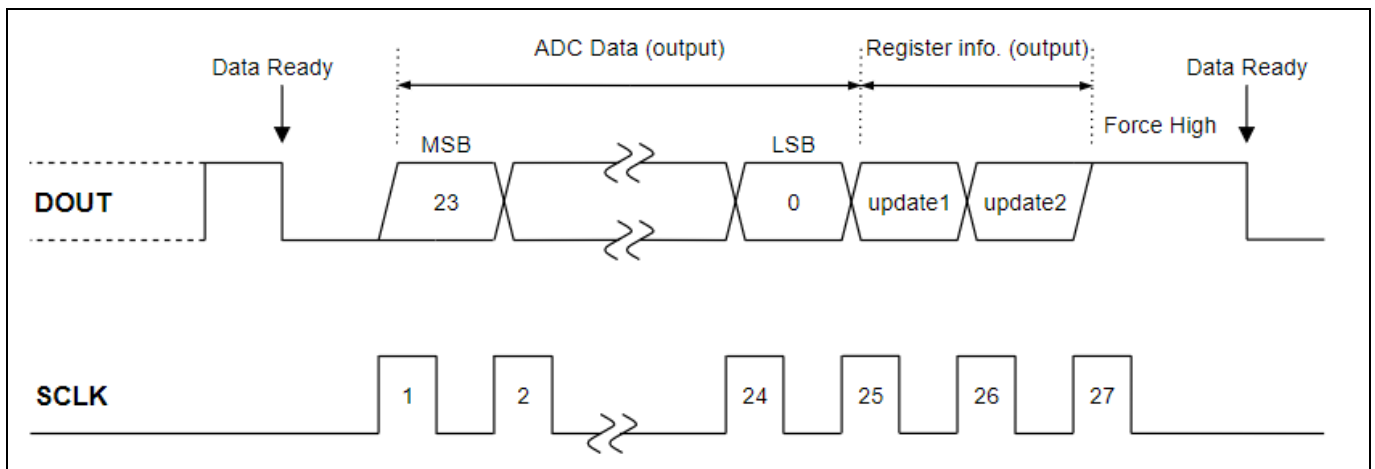


Fig. 9: Timing diagram of the reading data procedure (27 SCLKs).

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|--------------|---|-----|-----|-----|-------|
| T_{ds} | DOUT low to first SCLK rising edge | 0 | | | ns |
| T_{sclk} | SCLK positive or negative pulse width | 500 | | | ns |
| T_{pd} | SCLK rising edge to new data bit valid: propagation delay | 400 | | | ns |
| T_{ht} | SCLK rising edge to old data bit valid: hold time | 200 | | 400 | ns |
| T_{update} | Data updating: no read-back allowed | | 30 | | us |
| T_{conv} | Conversion time: (1/data rate), default=10Hz | | 100 | | ms |

Table 6: Read data timing table

5.6.7. Function Configuration

PMD040B can be configured with different functions through SCLK and DOUT. Figure 10 and Figure 11 shows the timing diagram of the function configuration.

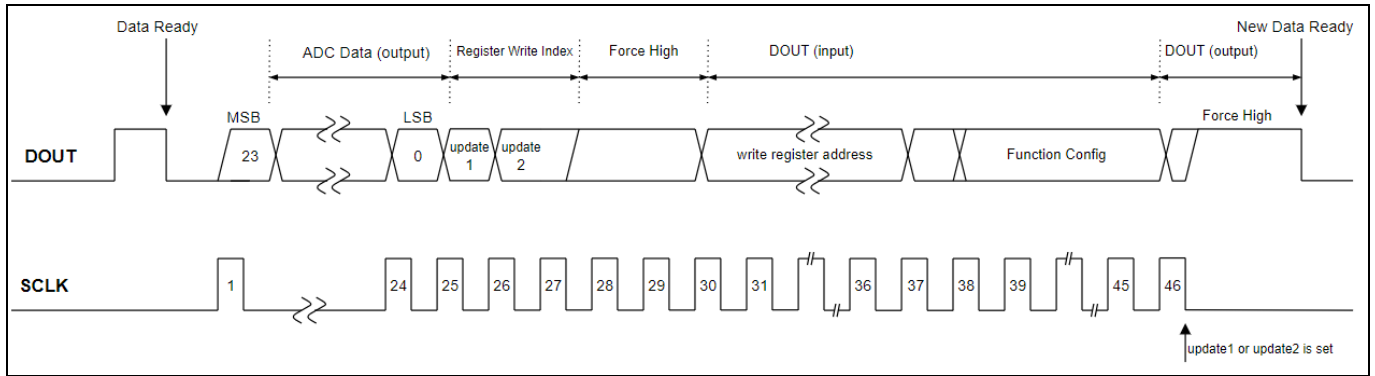


Fig. 10: Timing diagram of PMD040B configuration (write procedure).

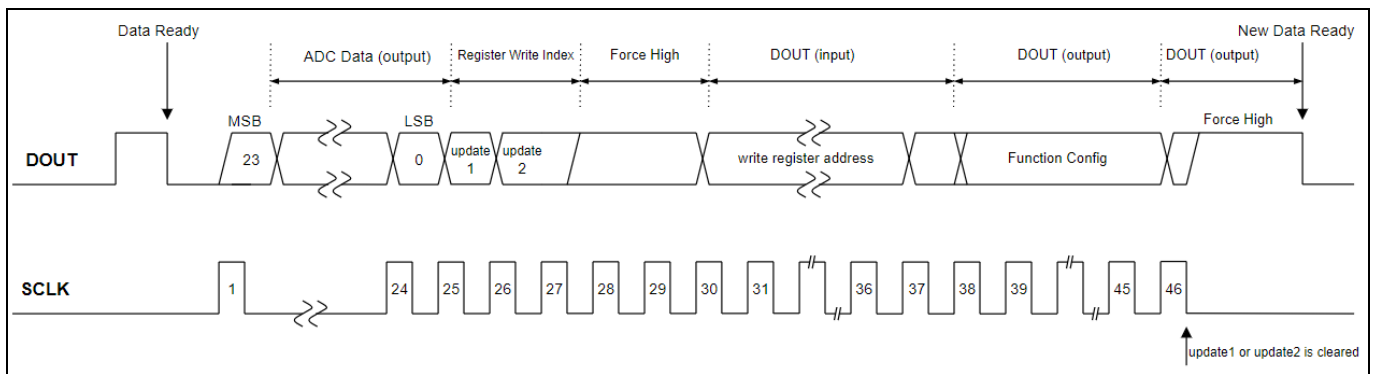


Fig. 11: Timing diagram of PMD040B configuration (read procedure).

Brief description of function configuration process of PMD040B is depicted below. After DOUT change state from high voltage level to low voltage level:

1. The 1st to 24th SCLK, read ADC conversion data. If the registers don't need to be configured or read, the following steps can be skipped.
2. The 25th to 26th SCLK, read the information if the register is updated.
3. The 27th SCLK, DOUT pull high.
4. The 28th to 29th SCLK, change DOUT as input pin.
5. The 30th to 36th SCLK, input the command to determine Read/Write and Register address. (high bit input first).
6. The 37th SCLK, change DOUT I/O direction. (If write register, DOUT is set input pin. If read register, DOUT is set output pin.)
7. The 38th to 45th SCLK, input register configuration data or output register configuration data. (high bit input/output first).
8. The 46th SCLK, change DOUT as output pin and pull DOUT to high level. The update1/update2 will be set or cleared.

5.6.8. SPI Command

PMD040B has 4 commands. The length of the command word is 7 bits. The description of commands is list below:

| command name | command words | SCLK | | | | | |
|-------------------------------|---------------|------------|------|------|-------------|------|------|
| | | command | | | Address | | |
| | | 30th | 31th | 32th | 33th | 34th | 35th |
| write configuration register1 | 0x61 | 6 (0b_110) | | | 1 (0b_0001) | | |
| write configuration register2 | 0x62 | 6 (0b_110) | | | 2 (0b_0010) | | |
| read configuration register1 | 0x51 | 5 (0b_101) | | | 1 (0b_0001) | | |
| read configuration register2 | 0x52 | 5 (0b_101) | | | 2 (0b_0010) | | |

Table 7: PMD040B command description table.

5.6.9. SPI Register Description

There are two registers that control the operation of PMD040B.

Configuration Register1 (cfgr1), address = 0b0001:

| Bit | Default | Name | Description |
|-------|---------|-----------|--|
| [7] | 0 | PWRSW_ENB | Power Switch ENB Control: 0: Power Switch Enable. 1: Power Switch Disable. |
| [6] | 0 | TS_DIFF | Temperature Sensor output switch. 0: VBEH → P VBEL → N 1: VBEH → N VBEL → P |
| [5] | 0 | TS_EN | Temperature Sensor Enable: 0: disable 1: enable |
| [4:2] | 000 | DSADC_DR | DSADC Output Data Rate Select: 000: 10Hz 001: 20Hz 010: 40Hz 011: 80Hz 100: 160Hz 101: 320Hz 110: 640Hz 111: 1280Hz |

PMD040B

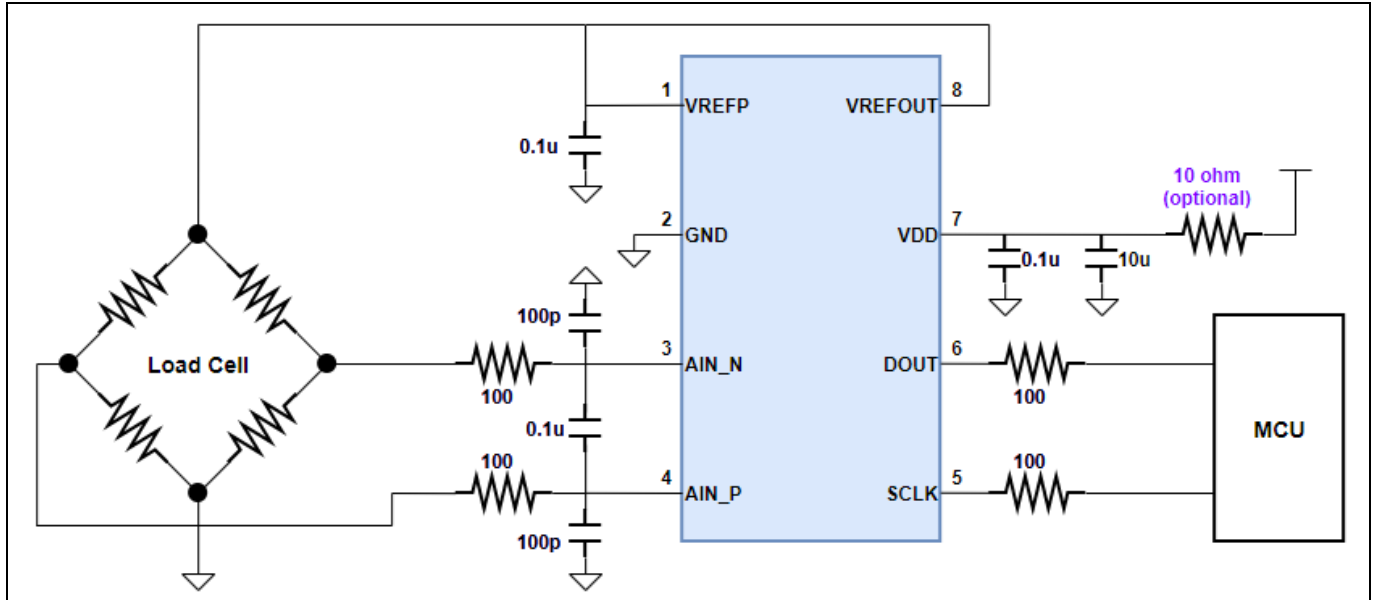
24-Bit Analog-to-Digital Converter

| Bit | Default | Name | Description |
|-------|---------|---------|---|
| [1:0] | 00 | MUX_SEL | MUX Input Measured signal source select: 00: ADC input. 01: Temperature Sensor input. 10: Internal Vref Test. 11: Input Short to VMID. |

Configuration Register2 (cfgr2), address = 0b0010:

| Bit | Default | Name | Description |
|-------|---------|-------------|---|
| [7:5] | 111 | PGA_GSEL | PGA Gain Select : 000 : x1 (not open) 001 : x2 (not open) 010 : x4 011 : x8 100 : x16 101 : x32 110 : x64 111 : x128 |
| [4] | 0 | PGABUF_GSEL | PGABUF Gain Select: 0: x1 1: x2 |
| [3] | - | - | - |
| [2] | 0 | - | - |
| [1] | 0 | - | - |
| [0] | 0 | PGA_BYPASS | PGA Bypass Select: 0: Normal mode. PGA+PGABUF+DSM 1: PGA off. PGABUF+DSM |

6. Application Circuit



Note: A 10ohm resistor connected in series with the power supply path can filter the power supply noise. This is optional.

7. Package

The PMD040B adopts SOP8 package.